Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A ferroelectric memory device, comprising:

a first bit line;

a second bit line;

a plurality of first memory cells each of which is connected to the first bit line, wherein each of the first memory cells includes one transistor and one ferroelectric capacitor;

a plurality of second memory cells each of which is connected to the second bit line, wherein each of the second memory cells includes one transistor and one ferroelectric capacitor;

a plurality of word lines each of which is connected to a respective one of the first and second memory cells;

a plurality of plate lines each of which is commonly connected to respective pairs of the first and second memory cells; [[and]]

a plurality of judgement memory cells each of which is connected between the first bit line and the second bit line, wherein each of the judgement memory cells includes two transistors and two ferroelectric capacitors; and

a plurality of judgement word line pairs each of which is connected to a respective one of the judgement memory cells, and wherein the judgement word lines of a respective judgement word line pair are supplied with a common voltage level.

Claim 2 (Canceled)

Claim 3 (Currently Amended): The ferroelectric memory device of claim 1, further comprising ~~a plurality of judgement word line pairs and~~ a plurality of judgement plate lines each connected to respective ones of the judgement memory cells.

Claim 4 (Currently Amended): The ferroelectric memory device of claim 3, wherein each of the judgement memory [[cell]] cells includes:

a first transistor which has a gate electrode connected to one judgement word line of a respective judgement word line pair, a first electrode connected to the first bit line and a second electrode;

a first capacitor connected between a respective judgement plate line and the second electrode of the first transistor;

a second transistor which has a gate electrode connected to [[the]] an other judgement word line of the respective judgement word line pair [[pairs]], a first electrode connected to the second bit line and a second electrode; and

a second ferroelectric capacitor connected between the respective judgement

plate line and the second electrode of the second transistor.

Claim 5 (Currently Amended): The ferroelectric memory device of claim 4, wherein each of the first memory cells includes a third transistor which has a gate electrode connected to a respective word line, a first electrode connected to the first bit line and a second electrode, and a third capacitor connected between a respective plate line and the second electrode of the third transistor, and

wherein each of the second memory cells includes a fourth transistor which has a gate electrode connected to [[a]] the respective word line, a first electrode connected to the second bit line and a second electrode, and a fourth capacitor connected between the respective plate line and the second electrode of the fourth transistor.

Claim 6 (Currently Amended): The ferroelectric memory device of claim 1, further comprising a plurality of digit line pairs and a plurality of gate transistor pairs, wherein each of the gate ~~transistors~~ transistor pairs connects a sense amplifier to a respective digit line pair.

Claim 7 (Currently Amended): A ferroelectric memory device, comprising:

a memory cell array which includes a plurality of first ferroelectric memory cells, wherein each first ferroelectric memory cell has a structure of one transistor and one capacitor;

a judgement memory cell array which includes a plurality of second ferroelectric memory cells, wherein each second ferroelectric memory cell has a structure of two transistors and two capacitors; [[and]]

a pair of bit lines; and

a plurality of judgement word line pairs, each of the judgement word line pairs being connected to respective ones of the second ferroelectric memory cells, wherein judgement word lines of a respective judgement word line pair are supplied with a same voltage level,

wherein the first ferroelectric memory cells in the memory cell array are alternatively connected to different [[each]] bit [[line]] lines of the bit line pair, and wherein the second ferroelectric memory cells in the judgement memory cell array are each connected to both bit lines of the bit line pair.

Claim 8 (Canceled)

Claim 9 (New): A ferroelectric memory comprising:

a memory cell array coupled to a bit line pair and including a plurality of memory cells, each of the memory cells having one transistor and one ferroelectric capacitor;

a judgement memory cell array coupled to the bit line pair and including a plurality of judgement memory cells, each of the judgement memory cells having first and second transistors and first and second ferroelectric capacitors; and

a plurality of judgement word line pairs, the judgement word line pairs being connected to respectively different ones of the judgement memory cells, and judgement word lines of respective judgement word line pairs are connected together.

Claim 10 (New): The ferroelectric memory of claim 9, further comprising a plurality of judgement plate lines coupled to respectively different ones of the judgement memory cells.

Claim 11 (New): The ferroelectric memory of claim 10, wherein each of the judgement memory cells is configured so that:

the first transistor has a first electrode connected to a first bit line of the bit line pair, a gate connected to a first judgement word line of a corresponding judgement word line pair, and a second electrode,

the first ferroelectric capacitor has a first electrode connected to the second electrode of the first transistor, and a second electrode connected to a corresponding judgement plate line,

the second ferroelectric capacitor has a first electrode connected to the corresponding judgement plate line, and a second electrode, and

the second transistor has a first electrode connected to the second electrode of the second ferroelectric capacitor, a gate connected to a second judegment word line of the corresponding judgement word line pair, and a second electrode connected to a

second bit line of the bit line pair.

Claim 12 (New): The ferroelectric memory of claim 9, wherein the memory cells include a plurality of first memory cells each connected to a first bit line of the bit line pair, and a plurality of second memory cells each connected to a second bit line of the bit line pair,

the first and second memory cells are coupled to respectively different word lines, and

respective pairs of the first and second memory cells are connected to respectively different plate lines.

Claim 13 (New): The ferroelectric memory of claim 12, wherein each of the first memory cells is configured so that the one transistor has a first electrode connected to the first bit line, a gate connected to one of the word lines, and a second electrode, and

the one ferroelectric capacitor has a first electrode connected to the second electrode of the one transistor, and a second electrode connected to one of the plate lines.

Claim 14 (New): The ferroelectric memory of claim 12, wherein each of the second memory cells is configured so that the one transistor has a first electrode connected to the second bit line, a gate connected to one of the word lines, and a second electrode, and

the one ferroelectric capacitor has a first electrode connected to the second electrode of the one transistor, and a second electrode connected to one of the plate lines.